Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A flash-memory peripheral comprising:
a local central processing unit (CPU) for executing instructions for operating the flash-memory peripheral;
a CPU bus primarily controlled by the local CPU;
a flash-serial buffer bus not primarily controlled by the local CPU;
a RAM buffer for storing flash data for storage by the flash-memory peripheral;
a flash-memory controller for controlling a flash memory that stores the flash data, having a slave port for coupling to the CPU bus and receiving commands from the local CPU, and having a master port for coupling to the flash-serial buffer bus for transferring flash data to the RAM buffer;
a serial link for connecting the flash-memory peripheral to a personal computer; and
a serial engine for sending and receiving the flash data serially over the serial link, the serial engine having a slave port for coupling to the CPU bus and receiving commands from the local CPU, and having a master port for coupling to the flash-serial buffer bus for transferring flash data to the RAM buffer;

wherein the flash data is read from the flash memory by the flash-memory controller and sent over the flash-serial buffer bus to the RAM buffer;

wherein the flash data is read from the RAM buffer through the flash-serial buffer bus to the serial engine to be sent serially over the serial link,

wherein incoming flash data is written to the RAM buffer through the flash-serial buffer bus from the serial engine,

wherein the incoming flash data is read from the RAM buffer through the flash-serial buffer bus to the flash-memory controller and written to the flash memory,

whereby the flash-serial buffer bus transfers the flash data and the CPU bus sends commands to the flash-memory controller and to the serial engine.

[c2] 2.The flash-memory peripheral of claim 1 further comprising:

a first slave port on the RAM buffer, for connecting the CPU bus to the RAM buffer;

a second slave port on the RAM buffer, for connecting the flash-serial buffer bus to the RAM buffer,

whereby the RAM buffer has two slave ports to connect to two buses.

[c3] 3.The flash-memory peripheral of claim 2 further comprising:

a read-only-memory ROM, coupled to the local CPU, for storing instructions to be executed by the local CPU including instructions to send commands to the flash-memory controller or to the serial engine.

[c4] 4.The flash-memory peripheral of claim 3 wherein the ROM is coupled to the local CPU through the CPU bus or through a ROM bus separate from the CPU bus.

[c5] 5.The flash-memory peripheral of claim 2 further comprising:
a flash memory for storing the flash data, the flash memory permanently connected to the flash-memory controller,
wherein the flash-memory peripheral is a flash drive.

[c6] 6.The flash-memory peripheral of claim 2 further comprising:
a slot for accepting a flash-memory card removably inserted by a user;
wherein the flash-memory controller is a flash-card controller connected to the slot;
wherein the flash-memory peripheral is a flash-card reader.

[c7] 7.The flash-memory peripheral of claim 2 further comprising:

a plurality of slots each for accepting a flash-memory card for storing the flash data;

a plurality of flash-card controllers, coupled to the plurality of slots to read flash-memory cards inserted into the plurality of slots, each flash-card controller having a slave port coupled to the CPU bus to receive commands from the local CPU, and each having a master port coupled to the flash-serial buffer bus, for transferring flash data to the RAM buffer,

wherein the flash-memory peripheral is a multi-slot flash-card reader.

[c8] 8.The flash-memory peripheral of claim 2 wherein the serial link is a Universal-Serial-Bus (USB).

[c9] 9.The flash-memory peripheral of claim 2 wherein the serial link is a IEEE 1394 bus, an Integrated-Device-Electronics (IDE) bus, a serial AT-attachment (SATA) bus, a PCI Express bus, or a mini-PCI Express bus.

[c10] 10.A flash reader comprising:

a local processor that executed instructions for controlling operation of the flash reader;

a processor bus, mastered by the local processor, for sending commands from the local processor;

a buffer bus, not connected to the local processor, for transferring flash data;

a RAM buffer for storing flash data;

a flash-memory controller for reading flash data from a flash memory in response to commands from the local processor;

a serial engine for sending the flash data as serial data over a serial interface;

a flash slave port, on the flash-memory controller, for connecting the flash-memory controller to the processor bus as a bus-slave device;

a flash master port, on the flash-memory controller, for connecting the flash-memory controller to the buffer bus when the flash-memory controller acts as a bus-master device;

an engine slave port, on the serial engine, for connecting the serial engine to the processor bus as a bus-slave device;

an engine master port, on the serial engine, for connecting the serial engine to the buffer bus when the serial engine acts as the bus-master device;

a first slave port, on the RAM buffer, for connecting the RAM buffer to the processor bus as a bus-slave device; and

a second slave port, on the RAM buffer, for connecting the RAM buffer to the buffer bus as a bus-slave device when the flash-memory controller or the serial engine acts as the bus-master device,

whereby the processor bus transfers commands while the buffer bus transfers the flash data bypassing the local processor.

[c11] 11.The flash reader of claim 10 wherein the processor bus acts independently of the buffer bus, the local processor able to send commands over the processor bus independent of and at a same time as flash data is transferred over the buffer bus.

[c12] 12.The flash reader of claim 11 wherein the local processor reads flash data from the RAM buffer, modifies the flash data, and writes modified flash data back to the RAM buffer, using the processor bus and the first slave port of the RAM buffer,
whereby the local processor can modify the flash data stored in the RAM buffer using the processor bus.

[c13] 13.The flash reader of claim 11 wherein the flash-memory controller is a first flash-card controller connected to a first slot for receiving a first flash-memory card that stores flash data;
further comprising:
a second flash-card controller connected to a second slot for receiving a second flash-memory card that stores flash data;
a second flash slave port, on the second flash-card con-

troller, for connecting the second flash-card controller to the processor bus as a bus-slave device;
a second flash master port, on the second flash-card controller, for connecting the second flash-card controller to the buffer bus when the second flash-card controller acts as a bus master device,
whereby multiple flash-cards can be read by flash reader.

[c14] 14.The flash reader of claim 11 wherein the RAM buffer stores pre-fetched blocks of the flash data read by the flash-memory controller into the RAM buffer before the serial engine requests the pre-fetched blocks,
whereby pre-fetched flash data is stored by the RAM buffer.

[c15] 15.The flash reader of claim 11 wherein the RAM buffer comprises:
a write buffer storing flash data from the serial engine for writing to the flash memory by the flash-memory controller;
a read buffer storing flash data from the flash memory written to the RAM buffer by the flash-memory controller.

[c16] 16.The flash reader of claim 15 wherein the write buffer and the read buffer are FIFO buffer regions in the RAM

buffer.

[c17] 17.The flash reader of claim 11 further comprising:
interface logic, coupled to the processor bus and coupled to the buffer bus, for connecting the processor bus or the buffer bus to an external RAM buffer for storing an overflow of flash data,
whereby overflow flash data is stored in the external RAM buffer.

[c18] 18.A flash device comprising:
processor means for executing controlling instructions;
first bus means for transferring commands from the processor means;
buffer bus means for transferring flash data that bypasses the processor means;
data buffer means, coupled to the buffer bus means as a bus slave, for storing flash data being read by the flash device;
flash-memory controller means, coupled to the first bus means as a bus slave, and coupled to the buffer bus means as a bus master, for controlling a flash memory and for reading flash data from the flash memory; and
serial engine means, coupled to the first bus means as a bus slave, and coupled to the buffer bus means as a bus master, for reading flash data stored by the data buffer means and for serially transmitting the flash data over a

serial link;

wherein the flash data is transferred from the flash-memory controller means to the data buffer means over the buffer bus means bypassing the processor means;

wherein the flash data is transferred from the data buffer means to the serial engine means over the buffer bus means bypassing the processor means,

whereby transfers of the flash data use the buffer bus means to bypass the processor means.

[c19] 19.The flash device of claim 18 wherein the buffer bus means is unconnected to the processor means, but the data buffer means is connected to the first bus means as a bus slave;

wherein the serial link is a Universal-Serial-Bus (USB), a IEEE 1394 bus, a PCI Express bus, or a mini-PCI Express bus.

[c20] 20.The flash device of claim 19 wherein the serial link connects to a personal computer that has a static random-access memory (SRAM) buffer for storing blocks of data generated by a CPU on the personal computer for transfer over the serial link and storage as flash data by the flash device.